REMARKS

Claims 1, 11-12, 16, and 20 are amended, claims 2-5 are canceled, and claims 24-26 are added; as a result, claims 1 and 6-26 are now pending in this application.

No new matter has been added through the amendments to claims 1, 11-12, 16, and 20. Support for the amendments to claims 1, 11-12, 16, and 20 is found throughout the specification, including but not limited to the specification at page 3, line 13 through page 5, line 14, and in FIGs. 2 and 3. Claim 11 has been amended merely to re-write claim 11 in independent form to include all of the limitations of the base claim from which claim 11 previously depended.

No new matter has been added through new claims 24-26. Support for the subject matter of new claims 24-26 is found for example, but not limited to, the specification at page 3, line 13 through page 5, line 14, and in claims 2-5 as originally filed in the application.

In the Drawings

The drawings were objected to under 37 C.F.R. § 1.83(a). Specifically, the Office Action states:[1]

> The drawings must show every feature of the invention specified in the claims. Therefore, the second transistor larger than the first transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
>
> Additionally there is no support in the drawings to show where the first circuit is size with respect to the second circuit.

Applicants respectfully suggest that the drawings do show all of the features included in the claims, and direct attention to the specification in the present application, which states:[2]

> Fig. 3 is a diagram 300 illustrating the relative size of the *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal-oxide semiconductor field-effect transistor 204, included in the inverter 200 shown in Fig. 2, in accordance with some embodiments of the present invention. Referring to Fig. 1, the first circuit 106 is sized with respect to the second circuit 108 such that for a pulse signal (shown in Fig. 4 and described below) applied at the input port 102, the transmitter 100 generates an output signal (shown in Fig. 4 and described below) having a rise-

[1] *See* the Office Action at page 5, lines 1-6.
[2] *See* the specification of the present application at page 4, lines 7-29.

> time and a fall-time that are substantially equal at the output port 104.
>
> Referring again to Fig. 1 and Fig. 2, in some embodiments, the sizing of the first circuit 106 includes sizing the *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal-oxide semiconductor field-effect transistor 204 included in the inverter 200. In some embodiments, the *n*-type metal-oxide semiconductor field-effect transistor 204 is sized to be larger than the *p*-type metal-oxide semiconductor field-effect transistor 202. Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 larger than the *p*-type metal-oxide semiconductor 202 compensates for a slow response in the second circuit 108.
>
> Referring again to Fig. 3, the diagram 300 includes an x-axis 302 and a y-axis 304. A physical layout illustration of the *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal-oxide semiconductor field-effect transistor 204 aligned along the x-axis is shown. The *p*-type metal-oxide semiconductor field-effect transistor 202 includes the gate 210, the drain/source 206, and the drain/source 218. The *n*-type metal-oxide semiconductor field-effect transistor 204 includes the gate 210, the drain/source 206, and the drain/source 220.

Further, the specification with respect to FIG. 4 states:[3]

> Fig. 4 is a diagram 400 showing a pulse signal 402 and an output signal 404 generated in response to the pulse signal 402 applied at the input port 102 of the transmitter 100, shown in Fig. 1.

Thus, Applicants submit that FIG. 1, FIG. 2, FIG. 3, and FIG. 4, at least when considered in combination, show that in some embodiments, the second transistor is larger than the first transistor, and also show that the first circuit (first circuit 106 including inverter 200 as further depicted in FIG. 3) is sized with respect to the second circuit such that for a pulse signal applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port of the transmitter. Thus, all the features of the pending claims are clearly depicted by the drawings.

In addition, it is respectfully noted that a schematic symbol, such as those used in FIG. 2 to represent transistors 202 and 204, are standard symbols recognized by those of ordinary skill in the art as being representative, in a general sense, of a wide variety of devices having a variety

[3] *See* the specification of the present application at page 5, lines 15-17.

of physical and electrical characteristics, and having a variety of operating parameters. For example, the transistor symbols used in FIG. 2 to represent devices 202 and 204 can be used to represent a wide variety of transistors having many different physical and electrical characteristics that are not specifically identified by the symbol itself.

However, in order to overcome this objection to the drawings, Applicants have submitted amended FIG. 2 with this response to include the phrase "IN SOME EMBODIMENTS, 204 IS SIZED TO BE LARGER THAN 202." No new matter is added through this amendment to FIG. 2. Support for this amendment is found, for example but not limited to, the specification at page 4, lines 18-20.

Applicants respectfully request withdrawal of the objection to the drawings.

Allowable Subject Matter

Claim 11 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 has been re-written in independent form to include all of the limitations of the base claim from which claim 11 previously and directly depended. Therefore, claim 11 is allowable.

New claims 24-26 depend from now independent claim 11, and include all of the subject matter included in independent claim 11, and more. Therefore, new claims 24-26 are allowable.

In addition, independent claim 16 has been amended to include the subject matter of claim 11 as claim 11 was pending prior to the amendments included with this response. Applicants submit that independent claim 16, and claims 17-19 that depend from independent claim 16, as least as now amended, are also allowable.

Applicants respectfully request reconsideration and allowance of claims 11, 16-19, and 24-26.

§103 Rejection of the Claims

Claims 1-10 and 12-15.

Claims 1-10 and 12-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Urakami et al. (U.S. Patent 6,794,909) in view of Arcoleo et al. (U.S. Patent 5,864,506). Applicants do not admit that Urakami et al. is prior art, and reserve the right to "swear behind" Urakami et al. as provided for under 37 C.F.R. § 1.131 at a later date. However, it is not necessary to swear behind Urakami et al. at this time because the claims are distinguishable over Urakami et al. in the proposed combinations suggested by the Office Action.

Claims 2-5 are canceled, so the rejection of claims 2-5 is moot. Applicants respectfully traverse the rejection of claims 1, 6-10, and 12-15.

Claims 1, 6-10, and 12-15 are not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.[4] because the proposed combination of Urakami et al. and Arcoleo et al. fails to disclose or suggest all of the subject matter included in any given one of claims 1, 6-10, and 12-15. By way of illustration, independent claim 1, as now amended, includes:

> a second circuit including a second circuit input port coupled to the output port of the first circuit, the second circuit including a second circuit output port coupled to an output port of the transmitter, **wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port of the transmitter.**

Thus, the first circuit in independent claim 1 is sized with respect to the second circuit such that for a pulse signal applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port of the transmitter. The Office Action relies on Urakami et al. as disclosing this subject matter of independent claim 1, but fails to point to any portion of Urakami et al. that discloses or suggests this.

[4] Applicants do not admit or agree that any proposed combination of Urakami et al. and Arcoleo et al. is possible.

Instead, the Office Action merely states,[5] "turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port." However, the Office Action fails to provide any support for this statement based on the specification of Urakami et al., or from any other evidence of record. Without such support, the statement appears to be unsubstantiated by the discussion of Urakami et al., and fails to provide a showing that meets the Office Action's burden to establish a *prima facie* case of obviousness with respect to independent claim 1.

In a further illustration of subject matter included in independent claim 1 and not disclosed or suggested by the proposed combination of Urakami et al. and Arcoleo et al., independent claim 1, as now amended, includes:

> a first circuit coupled to an input port of the transmitter, the first circuit including an input port and an output port and an inverter including no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor and a first gate of the first transistor and a second gate of the second transistor both coupled directly to the input port of the transmitter,
>
> wherein the first transistor and the second transistor of the inverter include a n-type metal-oxide semiconductor field-effect transistor connected in series with an p-type metal-oxide semiconductor field-effect transistor and **wherein the n-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the p-type metal-oxide semiconductor field-effect transistor.**
> (Emphasis added).

The Office Action admits that Urakami et al. fails to disclose wherein the second transistor is larger than the first transistor.[6] The Office Action relies on Arcoleo et al. as disclosing physical characteristics of transistors. However, there is no disclosure in the cited portion of Arcoleo et al. of an inverter wherein the n-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the p-type metal-oxide semiconductor field-effect transistor, as required by the subject matter of independent claim 1.

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[5] *See* the Office Action at page 6, at the last 6 lines on the page.
[6] See the Office Action at page 7, at the first two lines on the page.

Further, this subject matter of independent claim 1 is not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.. As noted in the specification of the application:[7]

> Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 larger than the *p*-type metal-oxide semiconductor 202 compensates for a slow response in the second circuit 108.

As further noted in the specification of the application:[8]

> As can be seen in the diagram 300, the length 308 of the *n*-type metal-oxide semiconductor field-effect transistor is about nine units, and the length 310 of the *p*-type metal-oxide semiconductor field-effect transistor is about three units. Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 at less than about two times the size of the *p*-type metal-oxide semiconductor field-effect transistor 202 may not provide sufficient compensation for a slow response in the second circuit 108. Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 at more than about three times the size of the *p*-type metal-oxide semiconductor field-effect transistor 202 may waste die real estate.

Thus, the subject matter of independent claim 1 provides one or more unexpected results, for example the output signal having a rise-time and fall time that are substantially equal at the output of the transmitter, in the combination as provided by independent claim 1. Therefore, independent claim 1 is not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.

For at least the reasons stated above, the proposed combination of Urakami et al. and Arcoleo et al. fails to disclose or suggest all of the subject matter included in independent claim 1, and so independent claim 1 is not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.

In another illustration of subject matter included in claims 1, 6-10, and 12-15 that is not disclosed or suggested by the proposed combination of Urakami et al. and Arcoleo et al., independent claim 12, as now amended, includes:

> wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port of the

[7] *See* the specification in this application at page 4, lines 20-22.
[8] *See* the specification in this application at page 5, lines 6-14.

> first circuit, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at an output port of the transmitter.

For reasons analogous to those stated above with respect to independent claim 1, independent claim 12 is not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.

Claims 6-10 and 13-15 depend from one of independent claims 1 and 12, and so include all of the subject matter included in the independent claim from which they depend, and more. For at least the reasons stated above with respect to independent claims 1 and 12, claims 6-10 and 13-15 are not obvious in view of the proposed combination of Urakami et al. and Arcoleo et al.

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 1, 6-10, and 13-15.

Claims 16-19.

Claims 16-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Urakami et al. (U.S. Patent 6,794,909) in view of Arcoleo et al. (U.S. Patent 5,864,506) in further view of Marshall et al. (U.S. Patent 6,876,224). Applicants do not admit that Marshall et al. is prior art, and reserve the right to "swear behind" Marshall et al. as provided for under 37 C.F.R. § 1.131 at a later date. However, it is not necessary to swear behind Marshall et al. at this time because the claims are distinguishable over Marshall et al. in the proposed combinations suggested by the Office Action.

Applicants respectfully traverse the rejection of claims 16-19.

As stated above, independent claim 16 has been amended to include the subject matter from claim 11. The subject matter of claim 11 was found to be allowable, at least in combination with the limitations from which claim 11 previously depended. Therefore, Applicants submit that independent claim 16, at least as now amended, and claims 17-19 that

depend from independent claim 16, are not obvious in view of the proposed combination of Urakami et al., Arcoleo et al., and Marshall et al.[9]

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 16-19.

Claim 20.

Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Urakami et al. (U.S. Patent 6,794,909) in view of Marshall et al. (U.S. Patent 6,876,224). Applicants respectfully traverse the rejection of claim 20.

Independent claim 20 is not obvious in view of the proposed combination of Urakami et al. and Marshall et al.[10] because the proposed combination of Urakami et al. and Marshall et al. fails to disclose or suggest all of the subject matter included in independent claim 20. By way of illustration, independent claim 20, as now amended, includes:

> a first circuit including a single and no more than one input port coupled to an input port of the transmitter and a single and no more than one output port
>
> wherein the first circuit includes an inverter including no more than two transistors including a n-type metal-oxide semiconductor field-effect transistor connected in series with an p-type metal-oxide semiconductor field-effect transistor, a first gate of the first transistor and a second gate of the second transistor both coupled directly to the input port of the transmitter, and wherein the n-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the p-type metal-oxide semiconductor field-effect transistor; and
>
> a second circuit including a single and no more than one second circuit input port directly coupled only to the single and no more than one output port of the first circuit, the second circuit including a second circuit output port coupled to an output port of the transmitter, wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port.

[9] Applicants do not admit or agree that any proposed combinations of Urakami et al., Arcoleo et al., and Marshall et al. are possible.
[10] Applicants do not admit or agree that any proposed combination of Urakami et al. and Marshall et al. is possible.

For reasons analogous to those stated above with respect to independent claims 1 and 12, Urakami et al. fails to disclose or suggest the subject matter included in independent claim 20. The addition of Marshall et al. fails to disclose or suggest the subject matter included in independent claim 20 and missing from Urakami et al. Thus, the proposed combination of Urakami et al. and Marshall et al. fails to disclose or suggest the subject matter of independent claim 20.

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of independent claim 20.

Claims 21-23.

Claims 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Urakami et al. (U.S. Patent 6,794,909) in view of Marshall et al. (U.S. Patent 6,876,224) in further view of Song (U.S. Patent 6,614,258).

Claims 21-23 depend from independent claim 20, and so include all of the subject matter included in independent claim 20, and more. Applicants believe they have established that any proposed combinations of Urakami et al. and Marshall et al. fail to disclose or suggest all of the subject matter included in independent claim 20. The addition of Song fails to remedy this deficiency in disclosing or suggesting the subject matter included in claims 21-23 and missing from Urakami et al. and Marshall et al.

Therefore, the proposed combination of Urakami et al., Marshall et al., and Song[11] fails to disclose or suggest all of the subject matter included in claims 21-23, and so claim 21-23 are not obvious in view of the proposed combination of Urakami et al., Marshall et al., and Song.

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 21-23.

Reservation of Rights

In the interest of clarity and brevity, Applicants may not have addressed every assertion made in the Office Action. Applicants' silence regarding any such assertion does not constitute any admission or acquiescence. Applicants reserve all rights not exercised in connection with

[11] Applicants do not admit or agree that any proposed combinations of Urakami et al., Marshall et al. and Song are possible.

this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicants do not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicants timely object to such reliance on Official Notice, and reserve all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicants reserve all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney (612-371-2132) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18th day of December 2007.

Name Amy Moriarty Signature